

Two-Dimensional Detector Arrays for Gamma Spectroscopy

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Abstract— We have developed a pixel detector hybrid called DANA-2 (Detector Array for Nuclear Applications). DANA-2 consists of a two-dimensional, monolithic Cadmium Zinc Telluride (CZT) detector array flip-chip bonded directly to a readout IC designed for high energy resolution. Both the detector and the IC have 16×16 pixels with a pitch of $0.5 \text{ mm} \times 0.5 \text{ mm}$; the detector thickness is 3 mm. Each readout channel features a low-noise, charge-sensitive input amplifier with continuous-reset feedback and two selectable energy ranges; a gain amplifier with a five-bit gain adjustment and eight-bit offset DAC; a shaper with eight selectable shaping times ranging from $0.5 \mu\text{s}$ to $4 \mu\text{s}$; a peak detector; and a trigger comparator. The data readout is controlled by a programmable token logic, which affords the user a high degree of flexibility in the selection of nearest-neighbor channels to be read out to account for charge sharing between pixels. To process the signals from the detector cathode, one of the readout channels, which is normally connected to a corner pixel, can instead be connected to the cathode through a dedicated I/O pad. The different characteristics of these cathode signals are accommodated through user configuration options for the signal polarity and input FET size. Other features of DANA-2 include the ability to disable the trigger on any channel and thus turn off “hot” pixels, and several test features such as an AC-coupled test signal input and the option to operate any peak detector in follower mode and connect it to the analog output to continuously monitor the shaper signal. We present below details of the DANA-2 design and first results from its performance characterization.

I. INTRODUCTION

SOLID-STATE pixel detector arrays, notably Cadmium Zinc Telluride (CZT) detectors, are increasingly being investigated for use in high-resolution gamma spectroscopy for applications such as homeland security and monitoring of special nuclear materials [1], as well as single-photon emission computed tomography (SPECT) and positron emission tomography (PET) [2] for medical imaging. This development has been aided by the advent of 3-D readout techniques [3] for CZT detectors, which have achieved energy resolutions better than 1% FWHM at 662 keV [4].

In most of these systems, the detector is connected to the readout IC through traces on a printed-circuit board or ceramic substrate. In an effort to avoid the charge loss and increased input capacitance associated with this approach, we have pursued the design of a 2-D hybrid pixel detector called DANA (Detector Array for Nuclear Applications). The first

version of DANA had some design problems, including poor power distribution, that prevented us from using it to acquire useful source spectra. To address these problems, we have recently developed DANA-2, the second version of this hybrid pixel detector.

In the 2-D pixel detector design the detector pixels are connected directly to the input pixel pads of a readout IC with matching channel pitch, using a suitable bump bonding technique. In this case the charge bundles created inside the solid-state detector are input directly into the readout IC's preamplifier through the bump bond. This technique results in ultra low input capacitance for small pixel sizes and avoids charge transport through a lossy medium such as a printed-circuit board. It therefore offers the potential for reducing noise and thus further improving the energy resolution that can be achieved with CZT pixel detectors.

DANA-2 is in effect a 2-D incarnation of the main signal processing chain of the one-dimensional RENA-3 [5]; it also takes heritage from an earlier 2-D pixel detector developed for x-ray astrophysics [6]. In addition to the lower input capacitance and noise that were already discussed, the advantages of this 2-D pixel detector include a fine pixel pitch (0.5 mm), more compact sensor-readout assembly, and ease of tiling array units into large-area 2-D arrays. On the other hand, its format entails the challenges of fitting the complex circuitry of the RENA-3 within each channel area, finding a solution for reliable, high quality and cost-effective IC-detector bonding, and having limited flexibility in choosing a pixel pitch once the readout design has been finalized.

In the following sections, we will discuss the design of the DANA-2 detectors and present first results acquired in testing these devices.

II. DESIGN OF THE DANA-2 DETECTORS

The DANA-2 pixel detector consists of a 16×16 array of channels with a pitch of $0.5 \text{ mm} \times 0.5 \text{ mm}$ that is flip-chip bonded to a spectroscopy-grade 2-D solid-state detector pixel array with matching pitch. Each channel provides a charge sensitive preamplifier followed by a gain stage and a shaper, a trigger comparator, a peak detector, and readout logic that allows for a maximum degree of flexibility in selecting the channels to be read. Fig. 1 shows a simplified block diagram of a readout channel on the DANA-2 IC. Key features of DANA-2 are summarized in Table I.

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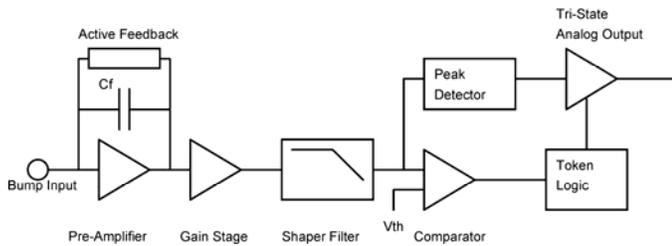


Fig. 1. Simplified block diagram of a readout channel on the DANA-2 IC.

Table I. Key features of the DANA-2 pixel detector.

Pixel geometry	$16 \times 16 = 256$, $0.5 \text{ mm} \times 0.5 \text{ mm}$ pitch
Front end	Self-resetting charge sensitive amplifiers
Input energy ranges	200 keV and 800 keV, user-selectable
Gain and offset	Digitally adjustable for each channel, five and eight bits, respectively
Pulse shaping time	Selectable for each channel, 0.5 to 4 μs
Input polarity	Positive and negative user-selectable
Cathode readout	Provision for cathode readout for pulse height ratio for correcting depth-of-interaction effect on energy resolution
Data readout	Controlled by programmable token logic, for maximum flexibility in channel selection
Connection	Daisy chain capability allows multiple ICs to share configuration and readout lines.
Test input	A test input allows IC testing and calibration without a detector
Die size	$8.58 \text{ mm} \times 9.54 \text{ mm}$

The charge-sensitive preamplifier's input circuits are optimized for a detector capacitance of 0.5 pF and accept signals of either polarity. Two signal ranges, 200 keV and 800 keV nominal, can be selected by switching the capacitors in the feedback path; this selection is common to all channels. The resistive feedback is provided by a transconductance amplifier whose transconductance is controlled by an externally supplied bias current, labeled I_{tau} . This allows us to vary the preamplifier's charge integration time on a continuous scale to match it to the characteristics of the detector signals being processed.

The gain stage that follows the input amplifier has digitally adjustable offset and gain settings to compensate for pixel-to-pixel differences of the detector signal and leakage current and for process variations that affect the uniformity of the channel response. The offset is controlled by an eight-bit digital-to-analog converter (DAC). The DAC step size is proportional to an externally supplied reference voltage, V_{RI} , with a nominal proportionality constant of 7.8 mV/V, which corresponds to a full-scale DAC range of 2 V_{RI} . The gain adjustment has five bits and a response function that can be approximated with an accuracy of a few percent as $\text{gain}(x) = a/(b - x)$. The range of nominal gain values is 4.7 to 9.7.

The shaper circuit provides eight peaking times that are individually selectable for each channel. The peaking times

range from approximately 0.5 μs to 2 μs when the 200 keV range is selected in the input amplifier, and up to 4 μs in the 800 keV range with its larger feedback capacitance; the exact values depend on the feedback control current I_{tau} .

The comparator threshold voltage, which is common to all channels, is provided externally. When a comparator fires, it sets a bit in the chip's 256-bit hit register; these bits are wired-OR'ed to generate the DANA-2 event trigger. To retrieve the hit pattern, the bits can be copied to a shadow register, from which they are shifted out through a 16-bit parallel bus. The same bus can be used to overwrite the shadow register, whose contents are then copied back to the hit register. For a sparse readout of just those channels that had a trigger, this step of writing to the register can be skipped. A token scheme is used to read out the peak detector signals. Under the control of a clock signal, the token is passed between those channels whose hit register bits are set, causing each corresponding peak detector in turn to be connected to the chip's differential analog output. To keep "hot" detector pixels from overwhelming the trigger and readout logic, which would make it impossible to acquire data from good channels, triggering can be disabled in any channel via a configuration bit. A token output pad allows passing the token between chips, effectively allowing multiple ICs to be accessed through shared readout lines. Similarly, the signal lines for configuration and access to the hit register can be shared with the help of a chip enable pin.

To facilitate spectroscopic techniques that rely on measuring the signals from the common detector cathode in addition to the anode signals (e.g., [3]), the cathode can be connected to one of the DANA-2 channels through a general I/O pad. Ideally, we would have used a dedicated extra channel for this purpose, but extraneous layout and fabrication constraints did not allow enough room for this extra channel in this first version. We plan to incorporate this feature in the next, larger (32x32-pixel) array version, DANA-3. Instead, in this version we used the channel in one of the corners of the 16×16 array. A configuration bit is used to switch the polarity of the comparator and peak detector to match the polarity of the cathode signal. Setting this bit also lowers the amplifier offsets by half the DAC range, to provide additional room for the signal pulses.

For test purposes, DANA-2 provides a test signal input that can be connected to the input transistors of any combination of channels through 75 fF capacitors. The shaper signal from any channel can be monitored by connecting it to the chip's analog output through the peak detector, which for this purpose can be operated in follower mode. Buffered test points connected to various points along the signal processing chain of one DANA-2 channel – at the outputs of the preamplifier, the gain stage, the shaper, and the trigger comparator – offer additional monitoring options.

The configuration of each DANA-2 channel is controlled by a 21-bit configuration register. To minimize the space requirements of the configuration logic, the registers for the

256 channels are concatenated into a single 5,376-bit serial shift register. For debugging purposes, the configuration data can be read back through one of the chip's I/O pad.

Fig. 2 shows the layout of the DANA-2 IC. The 16×16 array of channels forms an easily recognizable pattern in the upper part of the chip. Since the CZT detectors bonded to DANA-2 have a guard ring and are therefore wider than the 8 mm needed for the pixel array, the die itself can also be correspondingly wider. The extra area, located to the left of the array, is used mainly for additional supply lines to minimize voltage drops across the chip. The chip's 57 general I/O pads are located along the bottom edge of the die. The area between the channel array and these pads is used for global circuits – I/O drivers, configuration and readout control logic, and bias generation. The die size is 8.58 mm \times 9.54 mm. The IC is fabricated in a 0.6 μ m process and was packaged for testing in a 240-pin ceramic quad flat pack (CQFP).

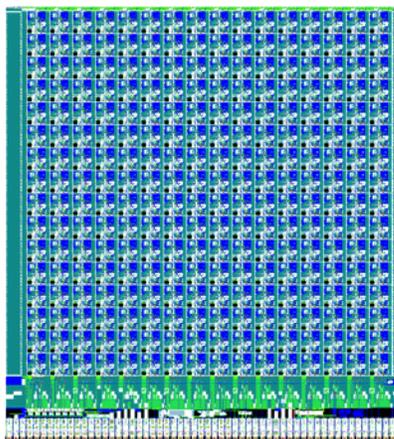


Fig. 2. Layout of the DANA-2 IC.

In producing the hybrid pixel detectors, we used 16×16 -pixel CZT detector arrays with a pitch of 0.5 mm in either direction. These arrays, which were manufactured by eV Products, are described in more detail in [7]. The pixel size is 0.4 mm \times 0.4 mm; the array is surrounded by a 0.17 mm wide guard ring. The resulting overall dimensions of the CZT crystal are 8.7 mm \times 8.7 mm; the detector thickness is 3 mm.

To facilitate testing of the detector arrays before they are bonded to readout ICs, the CZT crystals were mounted on ceramic substrates. Filled vias connect each detector pixel pad to the corresponding input pad on the readout chip. The ceramic extends beyond the crystal by 1.95 mm on one side. This overhang allows for easier handling of the arrays; it also provides room for a pair of guard ring connection pads.

The detector arrays were bonded to the ICs with a gold-stud bonding techniques. The gold studs were placed on the DANA-2 detector input pads before the chips were packaged for initial testing. For the actual bonding step, silver-filled epoxy was screen-printed onto the contact pads of the detector substrate to provide a conductive bond with the gold studs as soon as the detector was placed on top of the readout IC.

Fig. 3 shows a photograph of a detector array mounted on top of a chip inside a CQFP.

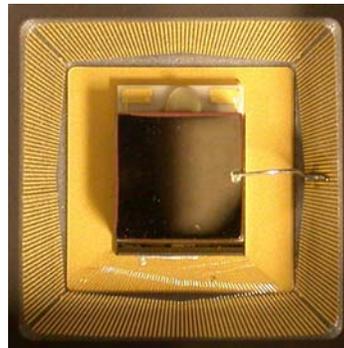


Fig. 3. Photograph of a CZT detector mounted on a readout IC inside a CQFP.

III. DANA-2 PERFORMANCE

To test the performance of DANA-2, we placed it in a test system that had been designed for the DANA and HILDA [8] pixel detectors. To provide a high degree of flexibility, the test system uses a motherboard/daughter board approach; a new daughter board was designed for DANA-2 to accommodate pinout differences between that chip and the original DANA. The hybrid detector is mounted in a commercial, off-the-shelf test socket on the daughter board. The test board provides the power, bias current and reference voltage supplies for the chip, as well as the detector bias voltage, and features a 14-bit analog-to-digital converter (ADC) to digitize the DANA-2 peak detector signals and a field-programmable gate array (FPGA) to control the IC configuration and readout. A DAC-controlled pulse generator is also provided. The test system is controlled from a PC via a bi-directional fiber-optic interface that uses a NOVA-designed PCI I/O board. Fig. 4 shows a photograph of the test board.

For a first test, we set the pulse generator on the test board to an amplitude of 5 fC and fed its signal into the DANA-2 channel that was equipped with multiple test points. We used a digital oscilloscope to record the signals from these test points for various configuration settings. Fig. 5 shows the signal observed at the test point for the preamplifier output, for different values of the feedback control current I_{tau} , in response to the falling edge of the test pulse signal. Increasing I_{tau} increases the feedback amplifier's transconductance, resulting in a faster decay of the preamplifier output pulse. The horizontal scale in Fig. 5 is 400 ns/div, the vertical scale is 20 mV/div. (Note, however, that the source followers used to buffer the test points introduce a gain – approximately 0.7, judging from the comparison of the shaper signals observed at the test point and at the chip's analog output – and offset.)

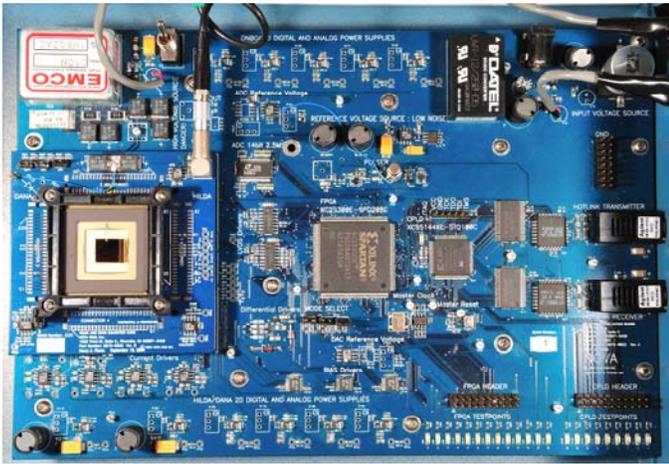


Fig. 4. Photograph of the HILDA/DANA(-2) test board, shown here with a HILDA daughter board.

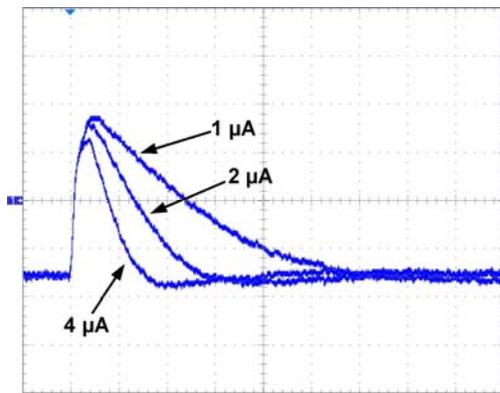


Fig. 5. Oscilloscope traces of the signal from the test point at the preamplifier output, for different values of the feedback control current I_{tau} . The oscilloscope's horizontal and vertical scales were set to 400 ns/div and 20 mV/div, respectively.

Fig. 6 shows signals from the gain stage test point for gain DAC settings of 0 (nominal gain 4.7), 15 (nominal gain 6.3), and 31 (nominal gain 9.7). The horizontal scale is 1 μ s/div, and the vertical scale is 100 mV/div. The observed pulse amplitudes scale reasonably well with the nominal gain values. Fig. 7 shows pulses from the shaper output for different values of the three control bits for the shaping time.

To test the offset adjustment DACs, we disabled the pulse generator and measured the voltage difference between the two pads of the differential analog output as a function of the DAC value. The transfer function of the output driver is such that this difference is the same as the offset between the signal baseline and the gain amplifier's reference voltage. Fig. 8 shows the measured offset as a function of the DAC value, for different values of VRI, the reference voltage that sets the DAC range. The amplifier started to saturate for offsets above 1.5 V, but below that voltage, the DAC response was highly linear, with a step size proportional to VRI.

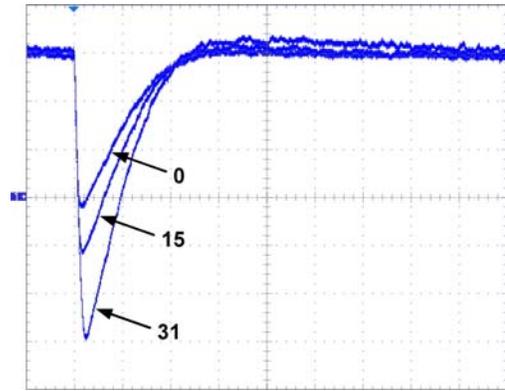


Fig. 6. Test point signal at the gain stage output for different gain DAC settings and $I_{tau} = 1 \mu A$. The oscilloscope's horizontal and vertical scales were set to 1 μ s/div and 100 mV/div, respectively.

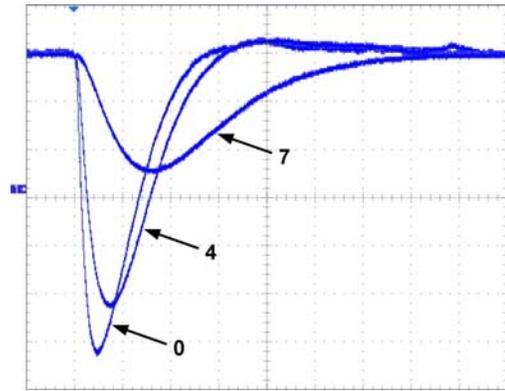


Fig. 7. Test point signal at the shaper output for different values of the shaper control bits, $I_{tau} = 1 \mu A$, and a gain DAC setting of 15. The oscilloscope's horizontal and vertical scales were set to 1 μ s/div and 100 mV/div, respectively.

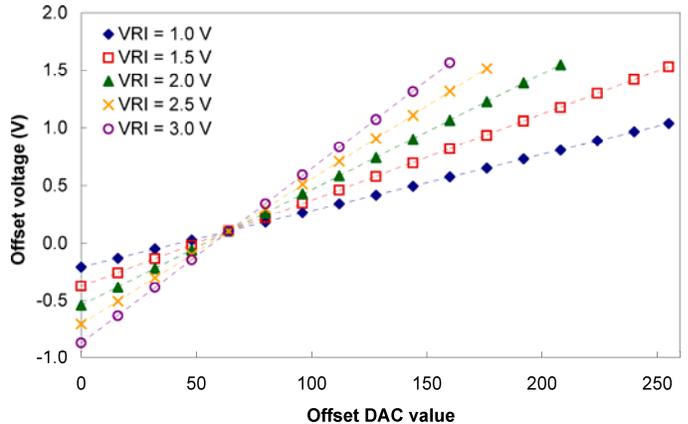


Fig. 8. DANA-2 offset voltage as a function of DAC value, for different values of the reference voltage VRI.

Sample test pulse spectra from one DANA-2 channel are shown in Fig. 9 for different input amplitudes. The input amplifier was set to the 800 keV range and the gain amplifier to a nominal gain of 6.3. The curves shown are Gaussian distributions fitted to the measured data.

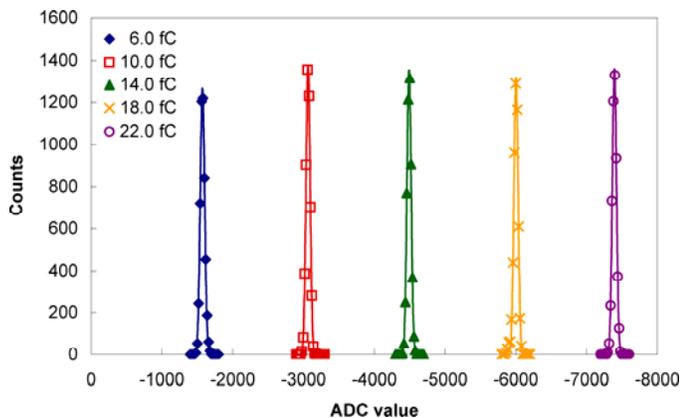


Fig. 9. Test pulse spectra from a DANA-2 channel, acquired for different pulse amplitudes. The input amplifier was set to the 800 keV range

The mean values obtained from the Gauss fits in Fig. 9, and from additional test pulse spectra for different amplitudes, are plotted in Fig. 10 as a function of the input amplitude. The dashed line shows the result of a linear fit to the measured data. The nonlinearity of the data shown here is approximately 0.9%.

We repeated this measurement for different gain settings of the amplifier gain stage and used the linear fit to determine the overall gain of the signal processing chain, from the preamplifier input to the ADC output, for each setting. The result is shown in Fig. 11, along with the curve representing the nominal gain values, which we scaled to match the data points. The scale factor was determined by a least-squares fit.

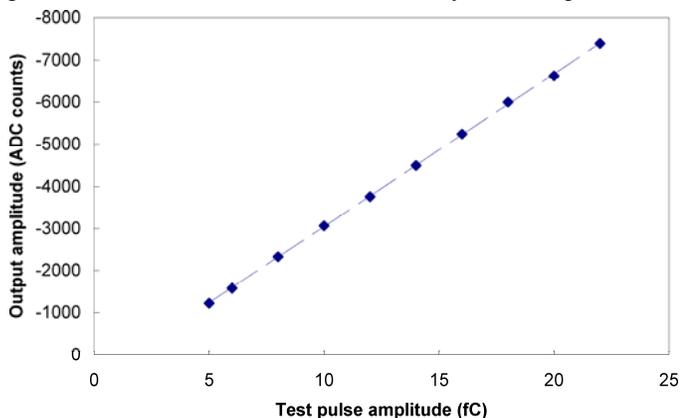


Fig. 10. Peak position of test pulse spectra as a function of pulse amplitude, for the 800 keV input amplifier range and a gain DAC setting of 15 (nom. gain 6.3).

After a CZT detector array had been bonded to the DANA-2 IC, we acquired spectra of ^{137}Cs , ^{22}Na , and ^{133}Ba sources. For these measurements, the detector was biased to 600 V, the DANA-2 input energy range set to 800 keV, and the gain to a nominal value of 6.3. The ^{137}Cs and ^{22}Na spectra from a pixel near the center of the detector are indicated in Fig. 12 by the blue and red curves, respectively. The ADC values extracted from these spectra for the 511- and 662-keV peaks and for the corresponding Compton edges (at 341 and 478 keV, respectively) are plotted in Fig. 13 as a function of these

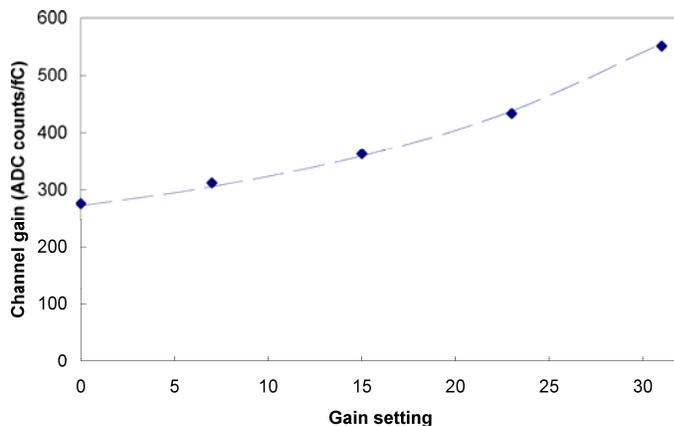


Fig. 11. The data points indicate the measured gain of the DANA-2 signal processing chain, including the ADC conversion gain, for different gain DAC settings. The dashed curve shows the nominal response of the gain stage, scaled to the measured data.

energies. The data points form a straight line, whose slope agrees within better than 10% with the slope shown in Fig. 10, if we use a value for the pair creation energy in CZT that falls within the generally accepted range of 4.5 to 5.0 eV per electron-hole pair. This agreement confirms the amplitude calibration of our pulse generator, which depends on the value of the DANA-2 test input capacitance; by extension, it also confirms that the true value of that capacitance is reasonably close to the nominal value of 75 fF.

We can also use the energy calibration provided by the data in Fig. 13 to estimate the FWHM energy resolution of the 511- and 662-keV peaks, 3.0% and 2.4%, respectively. This result is based on raw ADC data, without any depth-dependent pulse-height corrections.

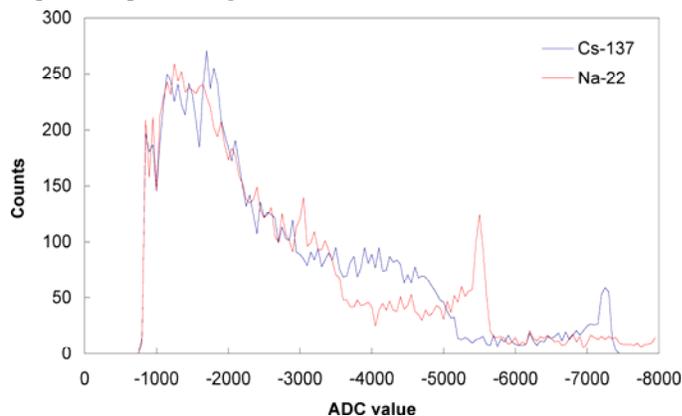


Fig. 12. Spectra of ^{137}Cs (blue) and ^{22}Na (red) from a pixel near the center of the DANA-2 pixel array. The 1275 keV line from ^{22}Na is beyond the detector's energy range.

The ^{133}Ba spectrum from the same pixel is shown in Fig. 14. The peaks corresponding to the 276-, 303-, 356-, and 384-keV lines are clearly discernible in the spectrum. The energy calibration obtained from these four lines is shown as an inset; it agrees within better than 2% with the calibration obtained from the spectra shown in Fig. 12.

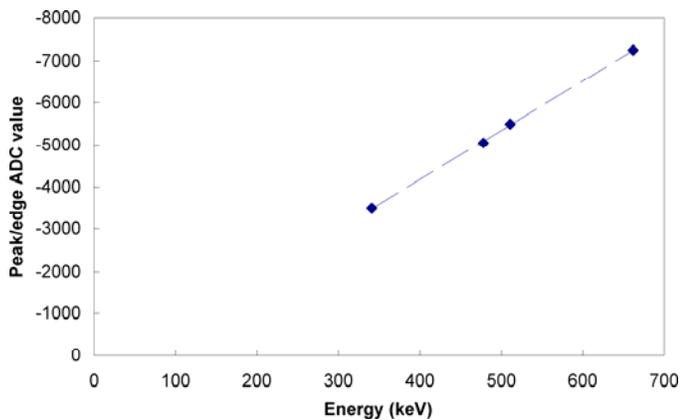


Fig. 13. Positions of the 511 keV and 662 keV peaks from the spectra in Fig. 12, as well as the corresponding Compton edges, as a function of the respective peak and edge energies. The dashed line represents a linear fit to the four data points.

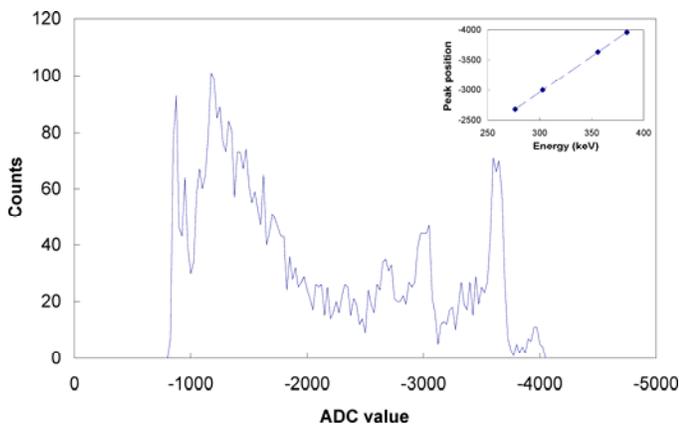


Fig. 14. Spectrum of ^{133}Ba , acquired from the same DANA-2 pixel as the spectra shown in Fig. 12. The inset shows the peak positions (ADC values) of the 276-, 303-, 356-, and 384-keV lines as a function of the gamma energy, and a linear fit to those data (dashed line).

IV. CONCLUSION

We have presented the design and initial test results for the DANA-2 pixel detector, which consists of a 3 mm thick 16×16 -pixel CZT detector array with 0.5 mm pixel pitch, flip-chip bonded to a matching readout IC. The initial performance data, including 2.4% FWHM energy resolution at 662 keV, are very encouraging; further improvements can be expected from optimizing details of the test system operation. For example, while the test socket used to hold the DANA-2 detectors offers a high degree of convenience, it also introduces additional noise through the extra leads and pressure contacts.

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